# REMARKS

This is a full and timely response to the non-final Office Action (Paper No. 6) mailed by the U.S. Patent and Trademark Office on October 23, 2002. Upon entry of the attached amendments, claims 1, 13, and 23 have been amended. Claims 1, 13, and 23 are hereby amended to more particularly point out and distinctly claim the subject matter that Applicant regards as the invention. No new matter is added. Reconsideration of the pending claims is respectfully requested, in view of the changes as denoted in the attached Appendix A and the following remarks. Each objection and rejection presented in the Office Action is discussed in the remarks that follow.

## I.  Response to Objection to the Specification

### A.  Statement of the Objection

The title of the invention is objected to for allegedly being non-descriptive of the claimed subject matter.

### B.  Discussion of the Objection - Title

Applicant has amended the title. Upon entry of the attached amendment the objection to the title is rendered moot.

## II.  Claim Objections

### A.  Statement of the Objection

Claim 3 is objected to because the phrase "propagated monotonically through said logic elements" is allegedly unclear.

### B.  Discussion of the Objection - Claim 3

Applicant respectfully traverses the objection of claim 3 for at least the reason that "monotonic progression" is a term-of-art used to describe digital-logic signal transfers within self-timed solid-state circuits. Such circuits use a transition-signaling protocol. Appendix B includes a copy of an article published by the Institute of Electronics and Electrical Engineers (IEEE) in November, 1991. Pages 1652-1653 describe a dual-monotonic function block. Appendix C includes a copy of a presentation on dynamic

circuits available on the Internet at "http://paradise.ucsd.edu/class/ece165/notes/lec7.pdf."
See slides 5-10 for a general description of pre-charged and pre-discharged logic gates
and evaluating digital logic upon detection of signals that rise and or fall monotonically.

Because the above-referenced documents indicate that one with ordinary skill in
the art would understand how "signals are propagated monotonically through said logic
elements," the meaning of the phrase as used in the context of claim 3 is clear.
Accordingly, Applicant respectfully requests that the objection of claim 3 be withdrawn.

### III.    Claim Rejections - Claims 1-23

#### A.    Statement of the Rejection

Claims 1-23 presently stand rejected under 35 U.S.C. §102(b) as allegedly
anticipated by Lesartre et al. (U.S. Patent No. 5,761,474 "the '474 patent.")

#### B.    Discussion of the Rejection - Claims 1-23

#### 1.    Claims 1-9

Applicant respectfully traverses the rejection of claims 1-9 under 35 U.S.C.
§102(b) for at least the reason that the cited reference fails to disclose, teach, or suggest
each method step in the claims.

It is well established that "anticipation requires the disclosure in a single prior art
reference of each element of the claim under consideration." *W.L. Gore & Associates,*
*Inc. v. Garlock, Inc.*, 721 Fed 2d 1540, 220 U.S.P.Q. 303, 313 (Fed Cir 1983). The
present rejection fails to meet the burden of identifying a single prior art reference that
discloses, teaches, or suggests each feature of the claimed invention.

Applicant's claimed invention is fundamentally different than the system and
method apparently disclosed in the '474 patent. As the title of the '474 patent indicates, it is
directed to operand dependency tracking to determine when it is appropriate to execute an
instruction in an out-of-order processor. In contrast, Applicant's claimed invention is
directed to an instruction reordering mechanism that causes a plurality of logic elements to
track which of the predefined plurality of said instructions are launched and causes the
selection of no more than said predefined number of ports during a launch cycle.
Identifying which instructions can be executed out-of-order based on operand dependencies,

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is <u>not</u> an instruction reordering mechanism that tracks which instructions are launched and causes the selection of no more than the predefined number of ports during the launch cycle.

For convenience of analysis, Applicant's independent claim 1, as amended, is repeated below in its entirety.

> 1. A method for finding a predefined plurality of instructions, if available, that are ready to be executed and that reside in an instruction reordering mechanism of a processor that can launch execution of instructions out of order via a predefined number of ports, comprising the steps of:
> (a) providing said instruction reordering mechanism having a plurality of said instructions, each said instruction having a respective logic element for causing and preventing launching, when appropriate, of said instruction; and
> (b) *propagating a set of signals successively during a launch cycle through said logic elements of said instruction reordering mechanism that causes said logic elements to track which of the predefined plurality of said instructions are launched and causes the selection of no more than said predefined number of ports during said launch cycle.*

(Applicant's independent claim 1 - *emphasis added*.)

The cited art of record fails to disclose, teach, or suggest at least the emphasized step of pending claim 1 as shown above. Consequently, claim 1 is allowable.

Specifically, the '474 patent fails to disclose, teach, or suggest Applicant's claimed *"propagating a set of signals successively during a launch cycle through said logic elements of said instruction reordering mechanism that causes said logic elements to track which of the predefined plurality of said instructions are launched and causes the selection of no more than said predefined number of ports during said launch cycle."* Accordingly, for at least this reason, Applicant's independent claim 1 is allowable.

Because independent claim 1 is allowable, dependent claims 2-9 which depend either directly or indirectly from claim 1 are also allowable. *See In re Fine*, 837, F.2d 1071, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988). Accordingly, Applicant respectfully requests that the rejection of claims 1-9 be withdrawn.

**2.      Claims 10-12**

Applicant respectfully traverses the rejection of claims 10-12 under 35 U.S.C. §102(b) for at least the reason that the cited reference fails to disclose, teach, or suggest each element in the claims.

For convenience of analysis, Applicant's independent claim 10 is repeated below in its entirety.

> 10.      A method for quickly finding a predefined plurality of instructions, if available, that are ready to be executed and that reside in a queue of a processor that can launch execution of instructions out of order, so that the found instructions can be communicated to a corresponding predefined plurality of ports associated with one or more execution resources, comprising the steps of:
>
> (a) providing said queue having a plurality of slots, each said slot for temporarily storing a respective instruction and launching, when appropriate, execution of said respective instruction; and
>
> (b) *propagating a set of signals successively through slots of said queue during a launch cycle that, when passed through a particular slot:*
>
> (1)    selects said particular slot for launching when said particular slot is ready by asserting in said slot one or more found signals that identify one or more specific ports associated with said one or more execution resources;
>
> (2)    refrains from selecting said particular slot when said particular slot is not ready by asserting in said slot a lost signal;
>
> (3)    *keeps track of how many slots have been selected during said launch cycle*; and
>
> (4)    *causes selection of no more than said predefined plurality of said instructions during said launch cycle.*

(Applicant's independent claim 10 - *emphasis added.*)

Applicant respectfully asserts that the cited art of record fails to disclose, teach, or suggest at least the emphasized step of pending method claim 10 as shown above. Consequently, claim 10 is allowable.

Specifically, the '474 patent fails to disclose, teach, or suggest Applicant's claimed step of *"propagating a set of signals monotonically through slots of said queue during a launch cycle that, when passed through a particular slot: . . . keeps track of how many slots have been selected during said launch cycle; and causes selection of no more than said predefined plurality of said instructions during said launch cycle."* Those portions of the '474 patent cited in the Office Action rejection describe how to determine when a particular instruction should not be executed (i.e., when there is a dependency upon a producer instruction). Consequently, the cited portions of the '474 <u>do not</u> disclose, teach, or suggest the emphasized step of independent claim 10. Accordingly, for at least this reason, Applicant's independent claim 10 is allowable.

Because independent claim 10 is allowable, dependent claims 11 and 12, which depend from claim 10 are also allowable. *See In re Fine, supra.* Accordingly, Applicant respectfully requests that the rejection of claims 10-12 be withdrawn.

### 3. Claims 13-22

Applicant respectfully traverses the rejection of claims 13-22 under 35 U.S.C. §102(b) for at least the reason that the cited reference fails to disclose, teach, or suggest each element in the claims.

For convenience of analysis, Applicant's independent claim 13, as amended, is repeated below in its entirety.

> 13.    A system for finding a predefined plurality of instructions, if available, that are ready to be executed in a processor that can launch execution of instructions out of order, comprising:
>> (a) an instruction reordering mechanism for temporarily storing a plurality of said instructions; and
>> (b) *a plurality of logic elements associated with said instruction reordering mechanism* and associated respectively with each of said instructions in said instruction reordering mechanism for causing and preventing launching, when appropriate, of respective instructions, *said logic elements configured to propagate a plurality of signals monotonically through said logic elements that causes said logic elements to select said predefined plurality of said*

> *instructions for launching and to de-select any*
> *remaining instructions during a launch cycle.*

(Applicant's independent claim 13 - *emphasis added.*)

Applicant respectfully asserts that the cited art of record fails to disclose, teach, or suggest at least the emphasized element and limitations of pending claim 13 as shown above. Consequently, claim 13 is allowable.

Specifically, the '474 patent fails to disclose, teach, or suggest Applicant's claimed *"plurality of logic elements associated with said instruction reordering mechanism . . . said logic elements configured to propagate a plurality of signals monotonically through said logic elements that causes said logic elements to select said predefined plurality of said instructions for launching and to de-select any remaining instructions during a launch cycle."* Accordingly, for at least this reason, Applicant's independent claim 13 is allowable.

Because independent claim 13 is allowable, dependent claims 14-22, which depend either directly or indirectly from claim 13 are also allowable. *See In re Fine, supra.* Accordingly, Applicant respectfully requests that the rejection of claims 13-22 be withdrawn.

### 4.    Claim 23

Applicant respectfully traverses the rejection of claim 23 under 35 U.S.C. §102(b) for at least the reason that the cited reference fails to disclose, teach, or suggest each element in the claim.

For convenience of analysis, Applicant's independent claim 23, as amended, is repeated below in its entirety.

23.    A system for finding a predefined plurality of instructions, if available, that are ready to be executed and that reside in a queue of a processor that can launch execution of instructions out of order, comprising:

(a) queue means for storing a plurality of said instructions, said queue means having a plurality of launch logic means for causing and preventing launching, when appropriate, of a respective instruction; and

(b) *logic means associated with said queue, said logic means for propagating during a launch cycle a set of signals monotonically to successive launch logic means to indicate both when and which of one or more ports of one or more execution resources are available for each said instruction and when none of said ports are available.*

(Applicant's independent claim 23 - *emphasis added.*)

Applicant respectfully asserts that the cited art of record fails to disclose, teach, or suggest at least the emphasized element of pending claim 23 as shown above. Consequently, claim 23 is allowable.

Specifically, the '474 patent fails to disclose, teach, or suggest Applicant's claimed "*logic means associated with said queue, said logic means for propagating during a launch cycle a set of signals monotonically to successive launch logic means to indicate both when and which of one or more ports of one or more execution resources are available for each said instruction and when none of said ports are available.*" Accordingly, for at least this reason, Applicant's independent claim 23 is allowable.
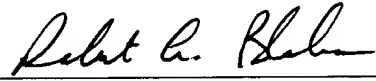
Accordingly, Applicant respectfully requests that the rejection of claim 23 be withdrawn.

## CONCLUSION

In summary, Applicant respectfully requests that the outstanding objection of claim 3 and the rejection of claims 1-23 be withdrawn. Applicant respectfully submits that presently pending claims 1-23 are allowable and the present application is in condition for allowance. Accordingly, a Notice of Allowance is respectfully solicited. Should the Examiner have any comments regarding the Applicant's response, Applicant requests that the Examiner telephone Applicant's undersigned attorney.

Respectfully submitted,

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